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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/817,193 | 03/27/2001 | Masahiko Tsuchiya | 108097 | 9085 |

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| EXAMINER |
|---|
| TRA, ANH QUAN |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 09/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/817,193 | TSUCHIYA, MASAHIKO | |
| | Examiner | Art Unit | |
| | Quan Tra | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 and 3-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-9* is/are rejected.

7)☒ Claim(s) *10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *15 & 18* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114 was filed in this application after appeal to the Board of Patent Appeals and Interferences, but prior to a decision on the appeal. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 03/24/2003 has been entered. A new ground of rejection is introduced as necessitated by amendment.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 3-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiozzi (USP 6060940) (newly cited) in view of Shulman (USP 6064258) (previously cited).

As to claims 1 and 7-9, Chiozzi shows in figures 1 a differential amplifier (the circuit figure 1 is semiconductor device, power supply circuit, or electronic equipment) comprising: a first differential amplifier circuit (16) having a first differential pair (differential pairs in 16 as shown) and operating based on a common input voltage (IN); and a second differential amplifier circuit (the lower differential amplifier circuit) having a second differential pair (as shown) and operating based on the common input voltage; a first current mirror circuit (as shown in 16)

provided in the first differential amplifier circuit and formed from a first transistor of a primary conductive type (p-channel) and a second transistor of the primary conductive type (p-channel); a second current mirror circuit (as shown in the lower differential amplifier) provided in the second differential amplifier circuit and formed from a first transistor of a secondary conductive type (n-channel) and a second transistor of the secondary conductive type (n-channel); a third transistor (10) of the primary conductive type having a gate connected to a first output line of the first differential amplifier; and a third transistor (18) of the secondary conductive type connected in series to the third transistor of the primary conductive type and having a gate connected to a second output line of the second differential amplifier circuit (as shown), wherein a third output line (OUT) connected between the third transistor of the primary conductive type and the third transistor of the second conductive type outputs an output voltage (OUT), and the first, the second, and the third output lines are shorted together via a first passive device (capacitor coupled between gate-drain of 10) coupled to the first output line and a second passive device (capacitor coupled between drain-gate of 18) coupled to the second output line. Thus, figure 1 shows all limitations of the claims except for at least one of the first differential pair and the second differential pair is formed from a pair of transistors having a driving ability difference therebetween. However, Shulman teaches in column 5 that the size of transistors in differential pair can be different in order to have off-set for the amplifier. Thus, it would have been obvious to one having ordinary skill in the art to make the size of transistors in Chiozzi's differential pair to be different for the purpose of having off-set for the amplifier.

As to claim 3, Chiozzi's figure 1 shows a fourth transistor (transistor in 16 that receiving signal IN) of the secondary conductive type connected in series to the first transistor of the

primary conductive type; and a fifth transistor (transistor in 16 that receiving signal OUT) of the secondary conductive type connected in series to the second transistor of the primary conductive type and having a driving ability different from the fourth transistor of the secondary conductive type (teachesin Shulman's column 5, lines 7-38), wherein the fourth transistor of the secondary conductive type and the fifth transistor of the secondary conductive type form the first differential pair.

As to claim 4, the combination fails to teach the driving ability of the fifth transistor of the secondary conductive type to be greater than the driving ability of the fourth transistor of the secondary conductive type. However, Shulman teaches the widths of the fourth and fifth transistors are adjusted to obtain the design current mismatch between the transistors. Therefore, it would have been obvious to one having ordinary skill in the art to selection of the driving ability of the fifth transistor of the secondary conductive type to be greater than the driving ability of the fourth transistor of the secondary conductive type for the purpose of to obtain the particular design current mismatch between the transistors.

As to claim 5, Chiozzi's figure 1 shows the second differential amplifier circuit includes: a fourth transistor (transistor, in the lower differential amplifier, that receiving signal IN) of the primary conductive type connected in series to the first transistor of the secondary conductive type; and a fifth transistor (transistor, in the lower differential amplifier, that receiving signal OUT) of the primary conductive type connected in series to the second transistor of the secondary conductive type and having a driving ability different from the fourth transistor of the primary conductive type (teaches by Shulman), wherein the fourth transistor of the primary

conductive type and the fifth transistor of the primary conductive type form the second differential pair.

As to claim 6, the combination fails to teach "a driving ability of the fifth transistor of the primary conductive type is set to be greater than a driving ability of the fourth transistor of the primary conductive type". However, Shulman teaches the widths of the fourth and fifth transistors are adjusted to obtain the design current mismatch between the transistors. Therefore, it would have been obvious to one having ordinary skill in the art to selection of the driving ability of the fifth transistor of the primary conductive type to be greater than the driving ability of the fourth transistor of the primary conductive type for the purpose of to obtain the particular design current mismatch between the transistors.

***Allowable Subject Matter***

4. Claims 10 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 10 would be allowable because the prior art fails to teach or suggest a circuit (such as figure 2) having the first output line (drain of 16) connected to the third output line (VOUT) through the first oscillation prevention capacitor (C1) and a first static electricity protection resistor (R1).

Claim 11 would be allowable because the prior art fails to teach or suggest a circuit (such as figure 2) having the second output line (drain of 36) connected to the third output line (VOUT) through the second oscillation prevention capacitor (C2) and a second static electricity protection resistor (R2).

***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
September 3, 2003

Quan Tra
Patent Examiner